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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,120	09/22/2003	Takashi Miyazawa	117244	5416

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/665,120	MIYAZAWA, TAKASHI	
	Examiner	Art Unit	
	STEPHEN G. SHERMAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,13,14 and 20-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13,14 and 20-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20 March 2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 14 May 2008 has been entered. Claims 1-8, 13-14 and 20-34 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-8, 13-14 and 20-34 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-8, 13-14, 20-26 and 28-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bae et al. (US 6,956,547) in view of Koyama (US 2002/0033783) and further in view of Dawson et al. (US 6,229,506).

Regarding claim 1, Bae et al. disclose an electronic circuit (Figure 7), comprising:

a first transistor that includes a first gate, a first drain and a first source (Figure 7 shows PM12 which has a gate, drain and source.),

a conduction state of the first transistor being set in accordance with a current signal supplied to a capacitor during a first period and a voltage signal supplied to the capacitor during a second period (Figure 7 shows that there is a current driver 310 and a voltage driver 340, where when the switch 330 allows the current driver 310 to be connected to the transistor PM14, i.e. a first period, then the conduction state of PM12 will be set in accordance with a current signal supplied through transistors PM14 and PM13 to capacitor C11, and where the switch 330 allows the voltage driver 340 to be

connected to the transistors PM14, i.e. a second period, then the conduction state of PM12 will be set in accordance with a voltage signal. See also column 9, lines 1-25.), and

a first current as the current signal flowing through the first transistor during at least a part of the first period (Column 9, lines 1-13 explain that transistors PM13 and PM14 are turned on, this means that the current flows to the capacitor C11 and transistors PM11 and PM12, which means that the current signal flows through PM12 during at least part of the first period.).

Bae et al. fail to teach a length of a third period, in which the conduction state of the first transistor set in accordance with the voltage signal, being changeable.

Koyama discloses an electronic circuit (Figures 15A and 15B) wherein the length of the period in which a voltage signal is supplied is changeable (Paragraph [0013] explains that a digital mode a voltage signal is supplied to the transistor 1515 shown in Figure 15B in order to produce digital gradation, while paragraph [0015] explains that a time-gradation mode is used to change the time during which a voltage signal is supplied.).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the digital gradation mode taught by Koyama in the electronic device taught by Bae et al. in such that the device would use the voltage driver for digital gradation in order to provide a display mode that can be used to supplement the current driving mode, which reduces variations in characteristics of the TFTs and obtains a uniform screen (See Koyama, first sentence of paragraph [0013]).

Bae et al. and Koyama fail to teach that an amount of charge in the capacitor being reset to a predetermined state when a second transistor is turned on.

Dawson et al. disclose an electronic circuit, wherein an amount of charge in a capacitor is reset to a predetermined state when a transistor is turned on (Figure 2, item 270; column 3, lines 20-22 and lines 44-52.).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to include a reset transistor as taught by Dawson et al. into the electronic circuit taught by the combination of Bae et al. and Koyama in order to reduce current nonuniformities and threshold voltage variations in a drive transistor (Dawson et al., column 2, lines 15-16).

Regarding claim 2, Bae et al., Koyama and Dawson et al. disclose the electronic circuit according to Claim 1.

Bae et al. also discloses the circuit further comprising:

a third transistor (Figure 7, PM14),

the current signal and the voltage signal being supplied to the capacitor through the third transistor (Figure 7 shows that the current driver 310 and the voltage driver 340 are connected to the capacitor C11 through PM14.).

Regarding claim 3, Bae et al., Koyama and Dawson et al. disclose the electronic circuit according to Claim 1.

Bae et al. also discloses the circuit further comprising:

a fourth transistor that controls an electronic connection between the first gate and the first drain (Figure 7 shows that PM13 controls the electrical connection between the first gate and the first drain of PM12.).

Regarding claim 4, Bae et al., Koyama and Dawson et al. disclose the electronic circuit according to Claim 1.

Bae et al. also disclose

a fifth transistor (Figure 7, PM11)

a second current whole level corresponds to the conduction state of the first transistor set in accordance with the current signal and the voltage signal (Figure 7 shows the circuit configuration such that a second current signal will exist which will correspond to the conduction state of the transistor PM12 and the amount stored in the capacitor C11.)

the fifth transistor controlling a timing to start or stop supply of the second current to an electronic element (Figure 7 shows the circuit configuration such that the transistor PM11 will control the second current signal that will flow the electronic element 101, and whether PM11 is on or off will determine if current will flow to the element 101.).

Regarding claim 5, Bae et al., Koyama and Dawson et al. disclose the electronic circuit according to Claim 1.

Bae et al. also disclose no current flowing through the first transistor during the third period (Column 9, lines 14-25 explain that when the voltage signal is supplied that PM12 is turned off, i.e. this means that no current is flowing through it.).

Regarding claim 6, please refer to the rejection of claim 1, and furthermore Bae et al. also disclose of a plurality of scanning lines (Figure 7 shows the scanning line connected to the gates of PM13 and PM14 and the gate driver unit 200, where it is inherent that in a display there will be a plurality of scanning lines.), a plurality of data lines (Figure 7 shows the data lines being connected to the source of PM14 and the switching 330, where it is inherent that in a display there will be a plurality of data lines.), a first circuit for outputting a current signal (Figure 7, current driver 310), and a second circuit for outputting a voltage signal (Figure 7, voltage driver 340).

Regarding claim 7, Bae et al., Koyama and Dawson et al. disclose the electro-optical device according to Claim 6.

Bae et al. also disclose the current signal and voltage signal being supplied to each of the plurality of unit circuits through one data line of the plurality of data lines (Figure 7 shows that the current driver 310 and the voltage driver 340 supply to the unit circuit through the data line described above.).

Regarding claim 8, Bae et al., Koyama and Dawson et al. disclose the electro-optical device according to Claim 6.

Bae et al. also disclose the plurality of data lines including a first data lines and a plurality of second data lines (Figure 7 shows that that from switch 330 there is a first line to current drier 310 and a second line to current driver 340.),

the current signal being supplied to each of the plurality of unit circuits through one first data line of the plurality of first data lines (Figure 7 shows the first line from current driver 310 to switch 330.); and

the voltage signal being supplied to each of the plurality of unit circuits through one second data line of the plurality of second data lines (Figure 7 shows the second line from voltage driver 340 to switch 330.).

Regarding claim 13, Bae et al., Koyama and Dawson et al. disclose the electro-optical device according to Claim 22.

Bae et al. also disclose the electro-optical element being an EL element (Column 9, line 10).

Regarding claim 14, Bae et al., Koyama and Dawson et al. disclose the electro-optical device according to Claim 13.

Bae et al. also disclose the EL element including a light-emitting layer that is composed of an organic material (Column 9, line 10).

Regarding claim 20, Bae et al., Koyama and Dawson et al. disclose an electronic apparatus, comprising: the electro-optical device according to Claim 6 (Figure 3 of Bae et al. or Figures 11A-11F of Koyama).

Regarding claim 21, Bae et al., Koyama and Dawson et al. disclose the electronic circuit according to Claim 1.

Bae et al. also disclose the current signal being a multi-valued data current (Column 9, lines 1-13).

Koyama also discloses the voltage signal being a binary data voltage (Paragraph [0013]).

Regarding claim 22, Bae et al., Koyama and Dawson et al. disclose the electro-optical device according to Claim 6.

Bae et al. also disclose each of the plurality of unit circuits including an electro-optical element (Figure 7 shows organic EL element 101.).

Regarding claim 23, please refer to the rejection of claims 1 and 4-5.

Regarding claim 24, please refer to the rejection of claim 23, where the first mode is a current mode corresponding to the first period, and the second mode is a voltage mode that corresponds to the second period.

Regarding claim 25, this claim is rejected under the same rationale as claim 21.

Regarding claim 26, this claim is rejected under the same rationale as claim 21.

Regarding claim 28, this claim is rejected under the same rationale as claim 2.

Regarding claim 29, this claim is rejected under the same rationale as claim 3.

Regarding claim 30, Bae et al., Koyama and Dawson et al. disclose the electronic circuit according to claim 1.

Bae et al. also disclose the electronic circuit further comprising:

an electronic element (Figure 7, element 101),

a second current whose current level corresponds to the conduction state of the first transistor being supplied to the electronic element (Figure 7 shows the circuit configuration such that a second current signal will exist which will correspond to the conduction state of the transistor PM12 and the amount stored in the capacitor C11, where the transistor PM11 will control the second current signal that will flow the electronic element 101.).

Regarding claim 32, this claim is rejected under the same rationale as claim 21.

Regarding claim 33, this claim is rejected under the same rationale as claim 21.

Regarding claim 34, Bae et al., Koyama and Dawson et al. disclose the electro-optical device according to claim 6.

Bae et al. also discloses a first electrode that is disposed opposite to a plurality of second electrodes, each of which is included in one electro-optical element of a plurality of electro-optical elements included in the plurality of nit circuits (Figure 7 shows that element 101 has a first electrode connected to VSS and a second electrode connected to PM11.).

Regarding claim 31, Bae et al., Koyama and Dawson et al. disclose the electronic circuit according to claim 34.

Bae et al. also discloses a potential of the first electrode being set at a constant during at least a part of a first period in which the current signal is supplied to the capacitor, and the potential of the first electrode being set at the constant during at least a part of a second period in which the voltage signal is supplied to the capacitor (Figure 7 shows that the first electrode of 101 is always connected to VSS, which means that it is connected to VSS during at least part of the first and second periods.).

6. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bae et al. (US 6,956,547) in view of Koyama (US 2002/0033783) and further in view of Dawson et al. (US 6,229,506) and Senda et al. (US 2002/0171607).

Regarding claim 27, Bae et al., Koyama and Dawson et al. disclose the electronic circuit according to Claim 24.

Bae et al., Koyama and Dawson et al. fail to explicitly teach of power consumption in the second mode being lower than a power consumption in the first mode.

Senda teaches switching between an analog image signal display, which is a first mode and a digital image signal display, which is a second mode. Senda teaches the second mode is lower in power consumption than in the first mode (Paragraph [0019], lines 1-6).

It would have been obvious for a person of ordinary skill in the art to have a power consumption in the second mode being lower than a power consumption in the first mode, as taught by Senda to the electronic circuit taught by the combination of Bae et al., Koyama and Dawson et al., so a to provide a device with power saving capabilities *(*Senda: Paragraph [0075]*)*.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN G. SHERMAN whose telephone number is (571)272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen G Sherman/
Examiner, Art Unit 2629

25 June 2008
/Bipin Shalwala/
Supervisory Patent Examiner, Art Unit 2629